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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/631,726	08/03/2000	Balaram Sinharoy	AT9-98-535	9223

7590 02/10/2005

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/631,726	SINHAROY, BALARAM	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 03 May 2004 and 27 September 2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been considered. Claims 6, 18, and 20 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 03 May 2004 and Amendment as filed 27 September 2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-18 and 20 are rejected under 35 U.S.C. 102(e) as being taught by Zuraski Jr. et al., U.S. Patent Number 6,502,188 (herein referred to as Zuraski).

5. Referring to claim 1, Zuraski has taught a method of generating a global history vector comprising the steps of:

a. Determining if a selected group of instructions contains a branch instruction (Zuraski column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67; column 11, lines 2-8; and Figure 1);

b. Maintaining a current global history vector in a shift register when the selected group does not contain a branch instruction (Zuraski column 2, lines 26-27;

column 4, lines 36-40; column 5, lines 23-67; and Figure 1). In regards to Zuraski, maintaining a current global history vector is inherent, since the vector is not changed in the shift register unless there is a branch.

c. Shifting a first value into the shift register to generate a second vector if the selected group contains a branch instruction and the branch instruction is predicted as a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5);

d. Shifting a second value into the shift register to generate a second vector when the selected group contains a branch instruction and the selected group does not include a branch instruction predicted as a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5).

6. Referring to claim 2, Zuraski has taught storing the generated value in an entry in a branch instruction queue associated with the selected group of instructions (Zuraski column 10, lines 5-6 and Figure 3).

7. Referring to claim 3, Zuraski has taught the step of correcting the generated vector upon a misprediction comprising the substeps of:

a. Retrieving a selected number of bits of the vector stored from the branch instruction queue into the shift register (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7); and

b. Shifting an updated history bit into the shift register (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7).

8. Referring to claim 4, Zuraski has taught wherein the first value comprises a logic 1 and the second value is a logic 0 (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5).

9. Referring to claim 5, Zuraski has taught wherein the selected group of instructions comprises eight instructions (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5).

10. Referring to claim 6, Zuraski has taught a method of performing branch predictions comprising the steps of:

a. Indexing a branch history table using a first global history vector associated with a first fetch group of instructions during a first fetch cycle (Zuraski column 1, lines 12-32; column 12, lines 25-32; and Figure 3);

b. Generating a second global history vector associated with a second fetch group of instructions (Zuraski column 13, line 37 to column 14, line 5; Figure 6; and Figure 7) comprising the substeps of:

i. Retaining the first vector when the first fetch group does not contain at least one branch instruction (Zuraski column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67; column 11, lines 2-8; and Figure 1);

ii. Appending a bit of a first value to the first vector when the first fetch group has at least one branch instruction predicted to be a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5);

iii. Appending a bit of a second value to the first vector when the first group contains at least one branch instruction and contains no branch instructions predicted to be a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5); and

c. Indexing the branch history table using the second global history vector during a second fetch cycle to retrieve a second branch prediction value (Zuraski column 1, lines 12-32; column 12, lines 25-32; and Figure 3).

11. Referring to claim 7, Zuraski has taught storing the first and second vectors in an entry of a branch history queue associated with the first fetch group (Zuraski column 10, lines 5-6 and Figure 3).

12. Referring to claim 8, Zuraski has taught

a. Detecting a branch misprediction based on the first prediction value (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7);

b. Retrieving the first and second vectors from the branch history queue; (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7)

c. Indexing the branch history table using the first vector to correct the first prediction value (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7); and

d. Appending a corrected bit to the second vector to generate a corrected branch history vector (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7).

13. Referring to claim 9, Zuraski has taught wherein said first fetch cycle precedes the second fetch cycle by three fetch cycles (Zuraski column 1, lines 13-20). In regards to Zuraski, the clock cycle is the shortest possible time interval a stage needs, which includes three fetch cycles.

14. Referring to claim 10, Zuraski has taught wherein said steps of indexing comprises the step of gating the vector with selected bits of a current instruction address (Zuraski column 12, lines 25-38).

15. Referring to claim 11, Zuraski has taught wherein said steps of gating comprise the steps of performing XOR operations (Zuraski column 12, lines 25-38).

16. Referring to claim 12, Zuraski has taught wherein said substeps of appending comprise the substeps of shifting a bit into a shift register storing the second vector (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5).

17. Referring to claim 13, Zuraski has taught branch processing circuitry comprising:

a. A shift register for storing a global history vector (Zuraski column 9, lines 64-67; column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5);

b. Control circuitry for selectively updating a first global history vector stored in said shift register (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5) operable to:

i. Determine if a selected group of instructions contains a branch instruction (Zuraski column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67; column 11, lines 2-8; and Figure 1);

ii. Maintain said first global history vector in said shift register when the selected group does not contain a branch instruction (Zuraski column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67; and Figure 1). In regards to Zuraski, maintaining a current global history vector is inherent, since the vector is not changed in the shift register unless there is a branch.

iii. Shift a first value into the shift register to generate a second vector if the selected group contains a branch instruction and the branch instruction is predicted as a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5); and

iv. Shifting a second value into the shift register to generate a second vector when the selected group contains a branch instruction and does not contain a branch instruction predicted as a branch taken.

18. Referring to claim 14, Zuraski has taught a branch history table and circuitry for generating an index to an entry in said branch history table using selected bits from a current address and selected bits of said first vector to retrieve a prediction value stored therein (Zuraski column 1, lines 12-32; column 12, lines 25-32; and Figure 3).

19. Referring to claim 15, Zuraski has taught circuitry for updating said second vector when said prediction value results in a misprediction comprising:

a. A queue for storing said first and said second vectors (Zuraski column 10, lines 5-6 and Figure 3);

b. Circuitry for accessing said vectors from said queue (Zuraski column 10, lines 5-6 and 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7);

c. Circuitry for indexing said branch history table with said first vector and updating a corresponding entry with a corrected prediction value (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7); and

d. Circuitry for updating a vector in said shift register with said second vector (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7); and

e. Circuitry for shifting the corrected prediction value into said shift register (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7).

20. Referring to claim 16, Zuraski has taught wherein said branch processing circuitry forms a portion of a single-chip microprocessor (Zuraski column 9, lines 61-63; Figure 1; and Figure 3).

21. Referring to claim 17, Zuraski has taught a processing system comprising:\

a. A microprocessor comprising:

i. A branch history table for storing branch prediction values (Zuraski column 9, lines 34-37; column 10, lines 28-32; and Figure 3);

ii. A global history shift register for storing a global branch history vector (Zuraski column 9, lines 64-67; column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5);

iii. Logic for generating an index to said branch history table and accessing prediction values stored therein using selected bits of a said branch history vector stored in said shift register (Zuraski column 1, lines 12-32; column 12, lines 25-32; and Figure 3); and

iv. Control circuitry for updating a said global branch history vector stored in said shift register and operable to:

(1) Retain a current vector stored in said shift register when a selected fetch group does not contain at least one branch instruction (Zuraski column 2, lines 26-27; column 4, lines 36-40; column 5, lines 23-67; and Figure 1). In regards to Zuraski, maintaining a current global history vector is inherent, since the vector is not changed in the shift register unless there is a branch.

(2) Shift a bit of a first value into said shift register to generate an updated vector when the selected fetch group has at least one branch instruction predicted to be a branch taken (Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5); and

(3) Shift a bit of a second value into said shift register when said selected fetch group contains at least one branch instruction and contains no branch instructions predicted to be a branch taken

(Zuraski column 12, lines 38-42; column 13, lines 7-36; Figure 4; and Figure 5).

22. Referring to claim 18, Zuraski has taught wherein said microprocessor further comprises:

a. A branch instruction queue having a plurality of entries each associated with a fetch group for storing at least first and second corresponding global history vectors (Zuraski column 10, lines 5-6 and Figure 3);

b. Circuitry for detecting a misprediction associated with a prediction value retrieved from said branch history table and corresponding to said first global history vector in said branch instruction queue (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7);

c. Circuitry for retrieving said first vector from said branch instruction queue and accessing a corresponding entry in said branch history table to correct said prediction value stored therein (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7); and

d. Circuitry for retrieving and modifying said second vector to generate a corrected vector in said shift register (Zuraski column 10, lines 49-51; column 13, line 26 to column 14, line 5; Figure 3; Figure 5; Figure 6; and Figure 7).

23. Referring to claim 20, Zuraski has taught wherein said fetch group comprises eight instructions (Zuraski column 4, lines 12-19).

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zuraski Jr. et al., U.S. Patent Number 6,502,188 (herein referred to as Zuraski) as applied to claim 17 above, in view of Jerry M. Rosenberg's Dictionary of Computers, Information Processing, and Telecommunications Second Edition ©1987 (herein referred to as Rosenberg). Zuraski has taught wherein said processing system further includes a bus (Zuraski column 3, lines 59-60 and Figure 1). Zuraski has not explicitly taught system memory coupled to said microprocessor. However, Zuraski has taught that the processor receives instructions from the bus interface unit (Zuraski column 3, lines 59-60). Rosenberg system memory coupled to said microprocessor (Rosenberg page 376, memory (M) (MEM)). A person of ordinary skill in the art at the time the invention was made would have recognized that the system memory stores instructions to the processor, thereby ensuring the instructions are present in the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the system memory of Rosenberg in the device of Zuraski.

Response to Arguments

26. Applicant's arguments filed 27 September 2004 have been fully considered but they are not persuasive.

27. Applicants argue in essence on page 8 "...Zuraski does not shift a '1' or a '0' in the shift register based on whether a group of instructions contains a branch instruction predicted as taken." This has not been found persuasive. In the lines cited in the above rejection, Zuraski shifts a '1' (a first value) into the global history register based on whether a branch instruction is

predicted taken or not (Zuraski column 12, lines 37-42). The branch instruction must first be detected out of a group of instructions in order for the branch taken prediction to be made.

28. Applicants argue in essence on pages 8-9 "...Zuraski does not shift a '1' or a '0' in the shift register based on whether a group of instructions does not include a branch instruction predicted as taken." This has not bee found persuasive. In the lines cited in the above rejection, Zuraski teaches that a '0' (a second value) is shifted into the global history register when the detected branch instruction is predicted not-taken (Zuraski column 12, lines 37-42). This means that "group of instructions does not include a branch instruction predicted as taken" since the branch in the group of instructions is predicted as not-taken instead of taken.

29. Applicants argue in essence on pages 9-10, 14, 19, and 21 "...Zuraski does not disclose indexing a branch history table using a global history vector associated with a group of instructions." This has not been found persuasive. The branch history table is a table, which stores branch history data and makes branch predictions based off this history data. The Global History (Zuraski Figure 3, element 205) receives the branch prediction and final execution results of a branch (Zuraski column 12, lines 57-63), tracks whether the prediction was correct or incorrect (Zuraski column 12, line 63 to column 13, line 6), and indexes the data to make a branch prediction (Zuraski column 12, lines 27-30). Also, there are two different groups of instructions that may be applied to the language "fetch group" in the claim, since, in the broadest interpretation, "fetch group" is merely a group of instructions that have been fetched. The first interpretation may be that the fetch group are the eight branch instructions whose predictions are represented in by the prediction bits in the global history register (Zuraski column 13, lines 8-25), since all of those instructions are fetched instructions. The second, more generic

application, is regarding groups of instructions in general, which are disclosed in Zuraski in column 14, lines 6-47 and are groups of eight instructions.

30. Applicants argue in essence on page 10 "...Zuraski does not append a bit of a value to a vector when a fetch group has at least one branch instruction predicted as taken." This has not been found persuasive. Please see above paragraph 29 in regards to the "fetch group" and paragraph 27 in regards to appending a value when a branch has been predicted taken.

31. Applicants argue in essence on page 11 "...Zuraski does not append a bit of a value to a vector when the fetch group contains at least one branch instruction and contains no branch instructions predicted to be a branch taken." This has not been found persuasive. Please see above paragraph 29 in regards to the "fetch group" and paragraph 27 in regards to the no branch instructions predicted as taken.

32. Applicants argue in essence on pages 11-12

> ...Examiner must provide a basis in fact and/or technical reasoning to assert that Zuraski inherently discloses retaining a current vector stored in the shift register when a selected fetch group does not contain at least one branch instruction.

33. This has not been found persuasive. Registers, such as the global history register, only modify and/or add data when some type of control signal tells it to. Heuring's Computer Systems Design and Architecture teaches this on page 535. The registers in Heuring only input or modify the data in the register when the write and enable control signals are active. The rest of the time, i.e. when the write and enable control signals are not active, the data is stagnant, i.e. it stays the same. In Zuraski, the only time the global history register is modified is when there

is a branch present in the group of instructions. All other times the register is not written to or enabled in any way, so the data stays the same.

34. Applicants argue in essence on pages 12-13, 14, 17, and 19 "...there is no language in the cited passage that discloses that the value generated based on whether a group of instructions includes or does not include a branch instruction predicted as taken is stored in line buffer 20." This has not been found persuasive. Zuraski states in column 10, lines 47-49 that the line buffer "stores a global history 234". The global history 234, as can be seen in Zuraski Figure 3, is the output from the GHSR, what the Examiner has been referring to as the global history register.

35. Applicants argue in essence on pages 13-14, 15. 16, 17, 18-19, 20, and 21

> ...Zuraski does not disclose shifting an updated history bit into the shift register...the Examiner has not cited to any passage in Zuraski that discloses retrieving a selected number of bits of a vector stored in line buffer 210 into the shift register.

36. This has not been found persuasive. Zuraski has taught right shifting the register, which retrieves the bit(s) that were previously discarded when the new predictions were shifted into the register, so a selected number of bits have been retrieved and stored in the line buffer. Also, Zuraski has taught modifying the data in the global history register to reflect corrections made to the branch prediction. Modifying something means changing its form. Shifting something means changing its form. Appending something means to fix something. In this case, Zuraski is changing the value at the very end of the register to the correct value.

37. Applicant argues in essence on pages 15 and 20 "...there is no language in the cited passages that a prediction value from global predictor storage 205 is used to detect a branch

misprediction". This has not been found persuasive. First, the claim language states "detecting a branch misprediction based on the first prediction value." This implies that the branch misprediction is a result from the first prediction value being incorrect, which Zuraski reads upon. Second, the prediction value must be used to detect a branch misprediction. For a branch midprediction to be detected, it must be determined whether the branch prediction value and the actual branch prediction value are the same.

38. Applicant argues in essence on page 16 "The language in the cited passage is no specific as to a number of fetch cycles. Neither is there any language in the cited passage disclosing a number of three fetch cycles between a first fetch cycle (used to retrieve a first prediction value) and a second fetch cycle (used to retrieve a second prediction value). First, a superscalar design, such as that disclosed in Zuraski, chooses the shortest possible clock cycle (Zuraski column 1, lines 13-20), which could be three fetch cycles. There is nothing in the claim to limit how "fetch cycles" is read. So to read "fetch cycle" as indicated in the parentheses after the first and second fetch cycles would be reading limitations unto the claims, which are not present in the claims. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

39. Applicant argues in essence on pages 17-18 "...there is no language in the cited passages that discloses accessing vectors from a queue." This has not been found persuasive. Zuraski in

column 12, line 57 to column 13, line 6 has taught the update logic in Figure 3, elements 200 and 202 access the line buffer, which is similar to a queue.

Conclusion

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

41. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

44. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
7 February 2005

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